5719808

O.G. FIG. CLASS SUBCLASS APPROVED BY DRAFTSMAN

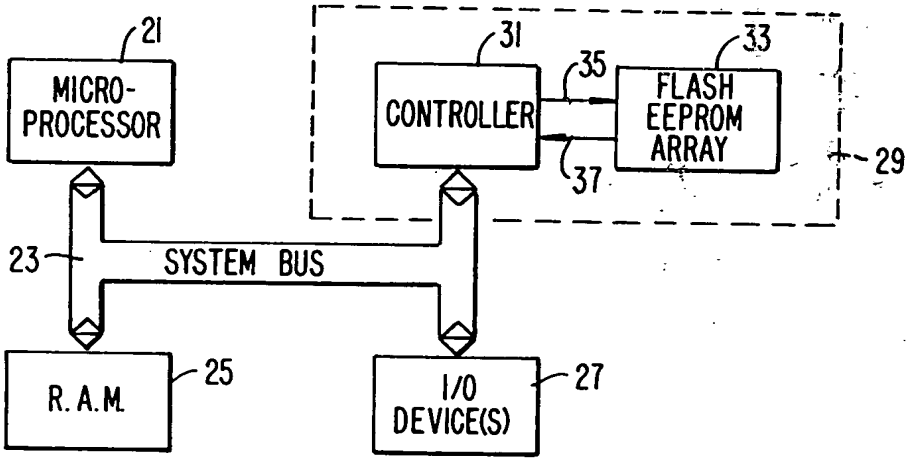


FIG._1A.

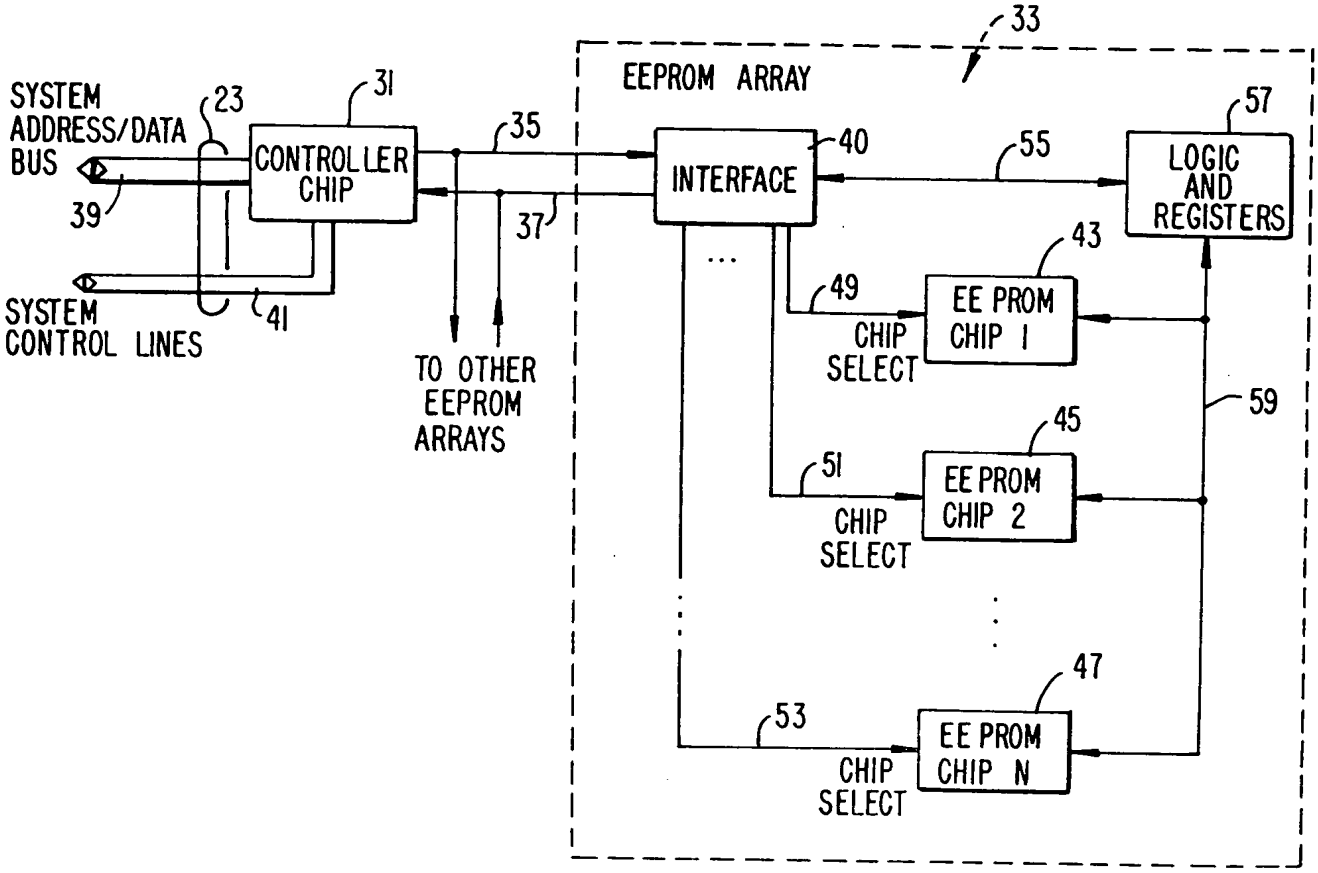


FIG._1B.

O.G. FIG. 3A
CLASS 365
SUBCLASS 185.33
APPROVED BY DRAFTSMAN

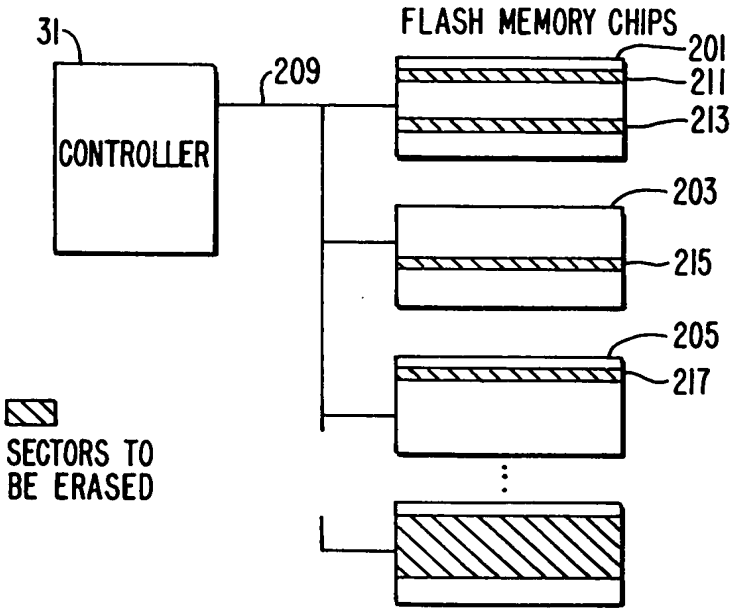


FIG._2.

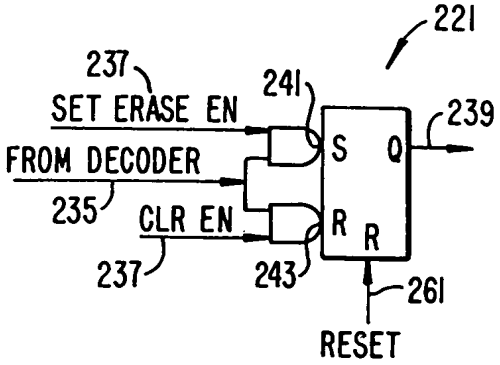


FIG._3B.

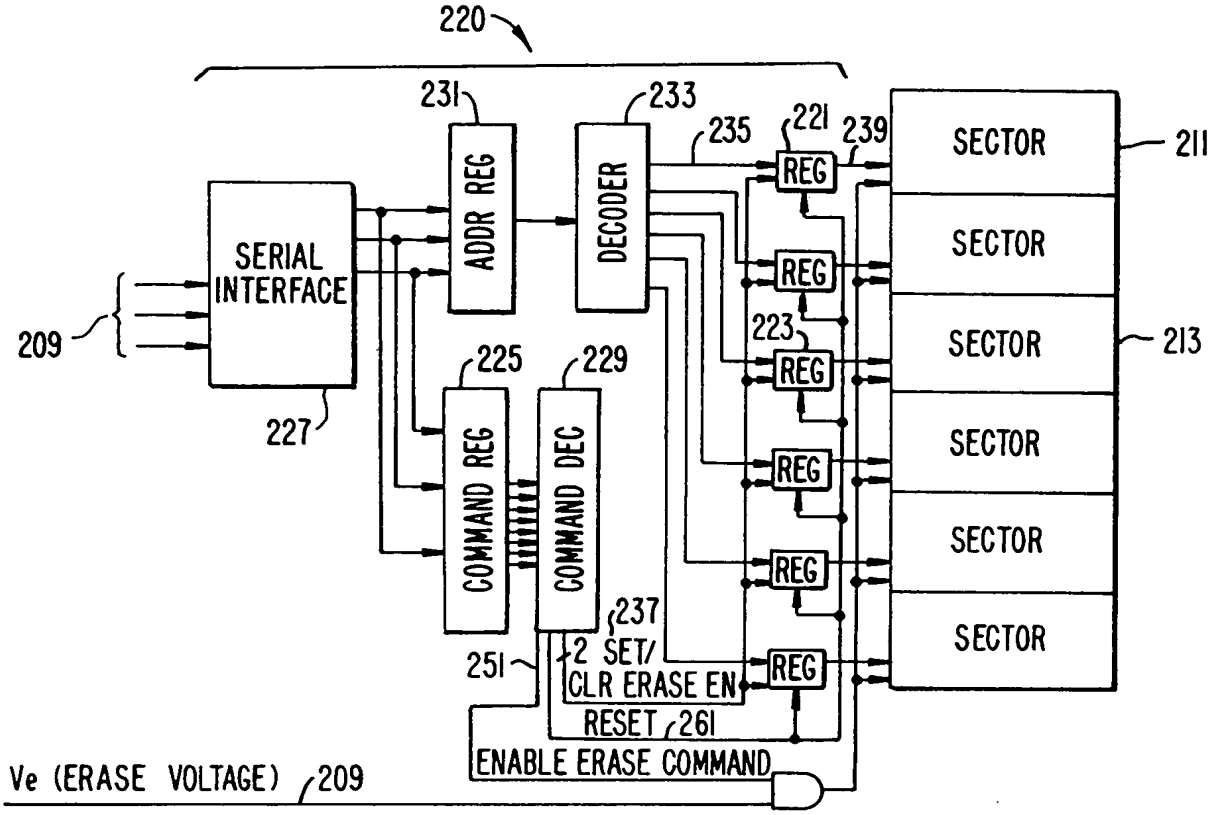


FIG._3A.

APPROVED BY DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS

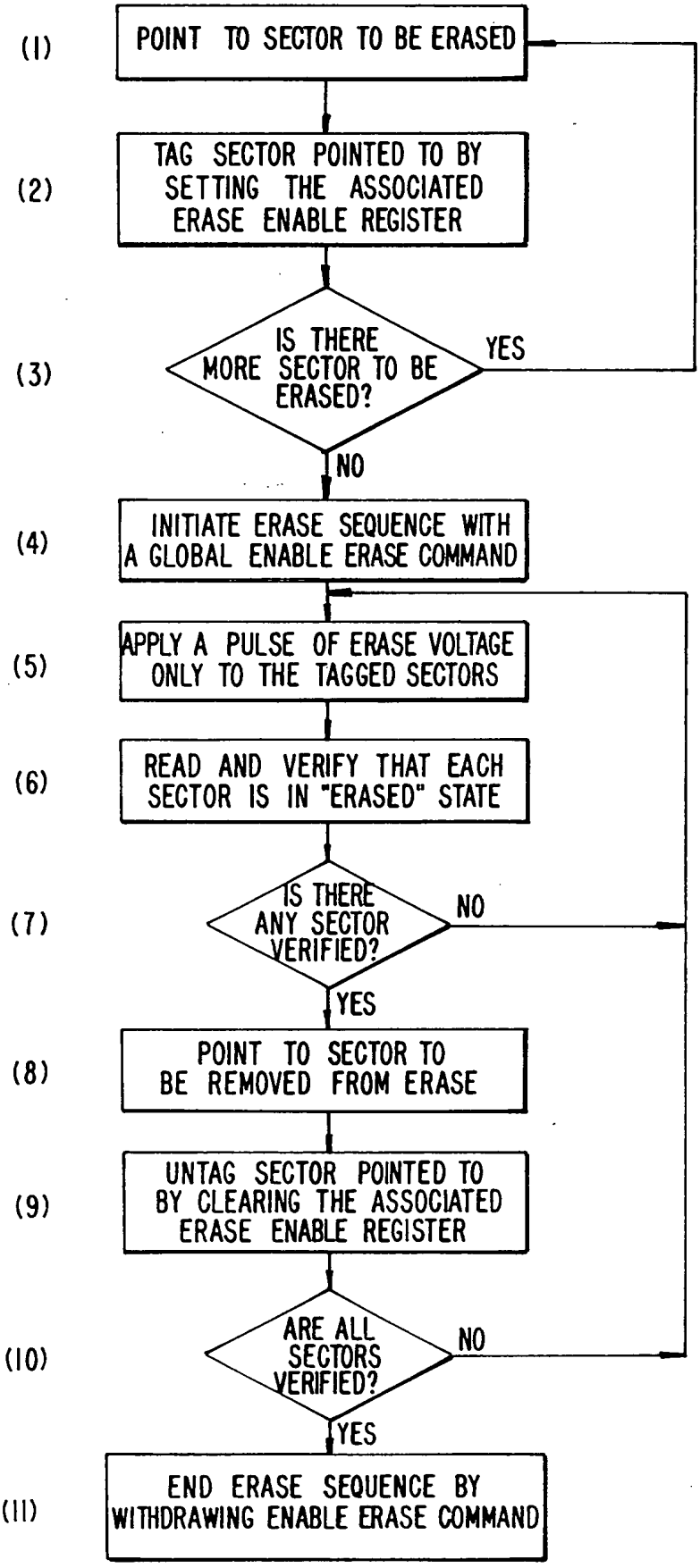
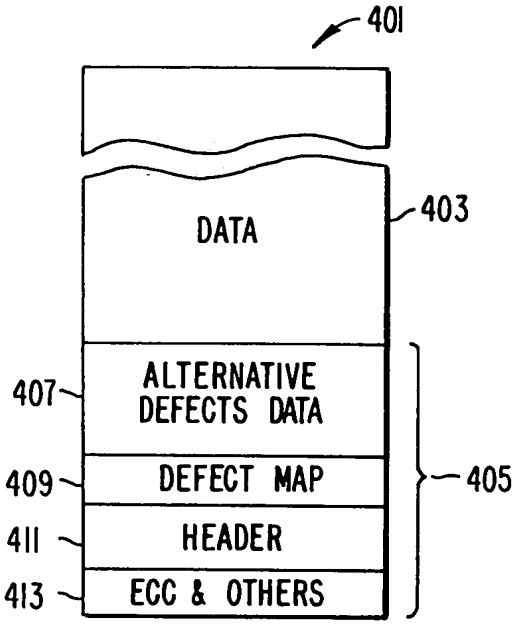


FIG._4.

APPROVED BY DRAFTSMAN O.G. FIG. CLASS SUBCLASS



SECTOR PARTITION

FIG._5.

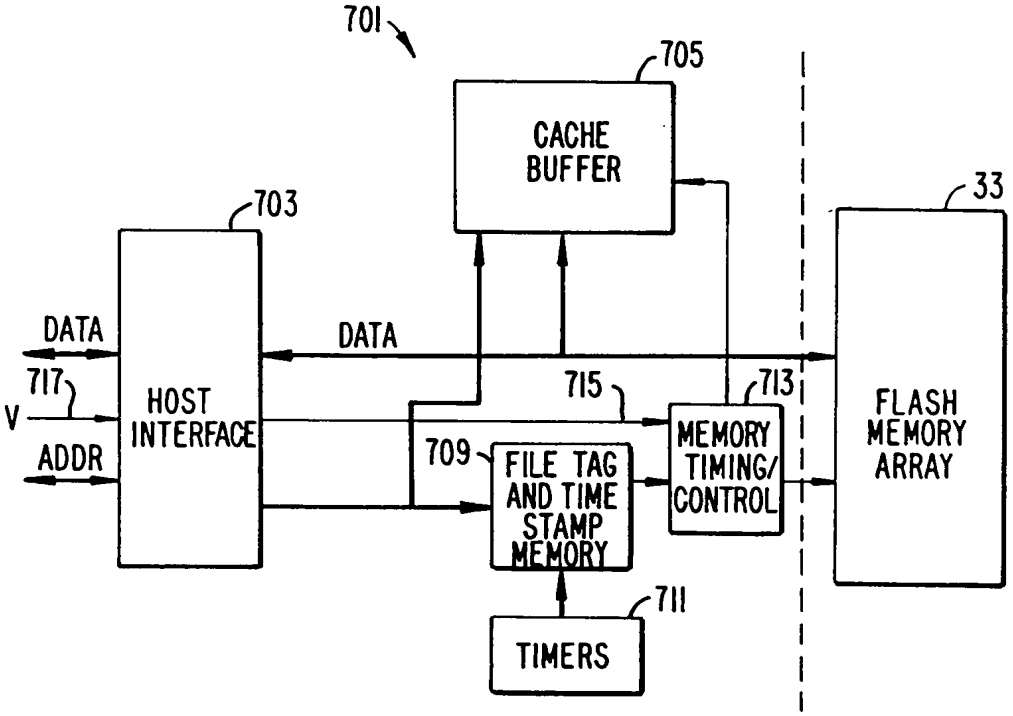
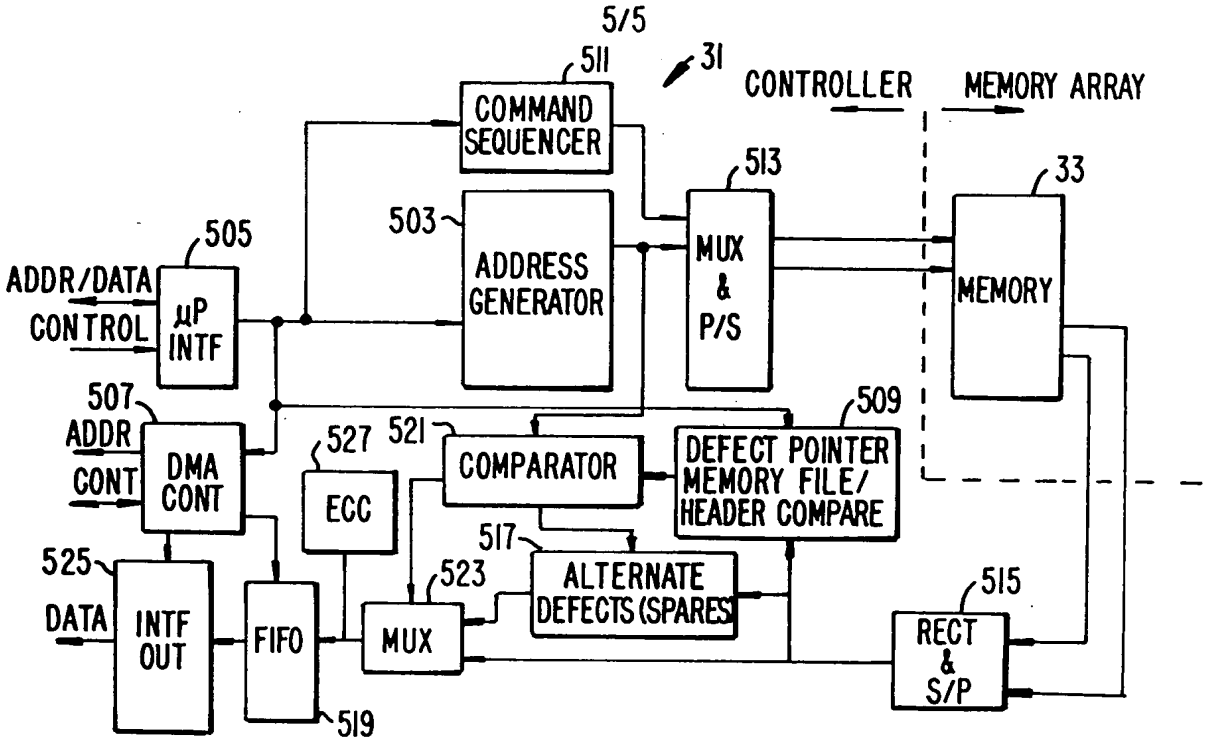


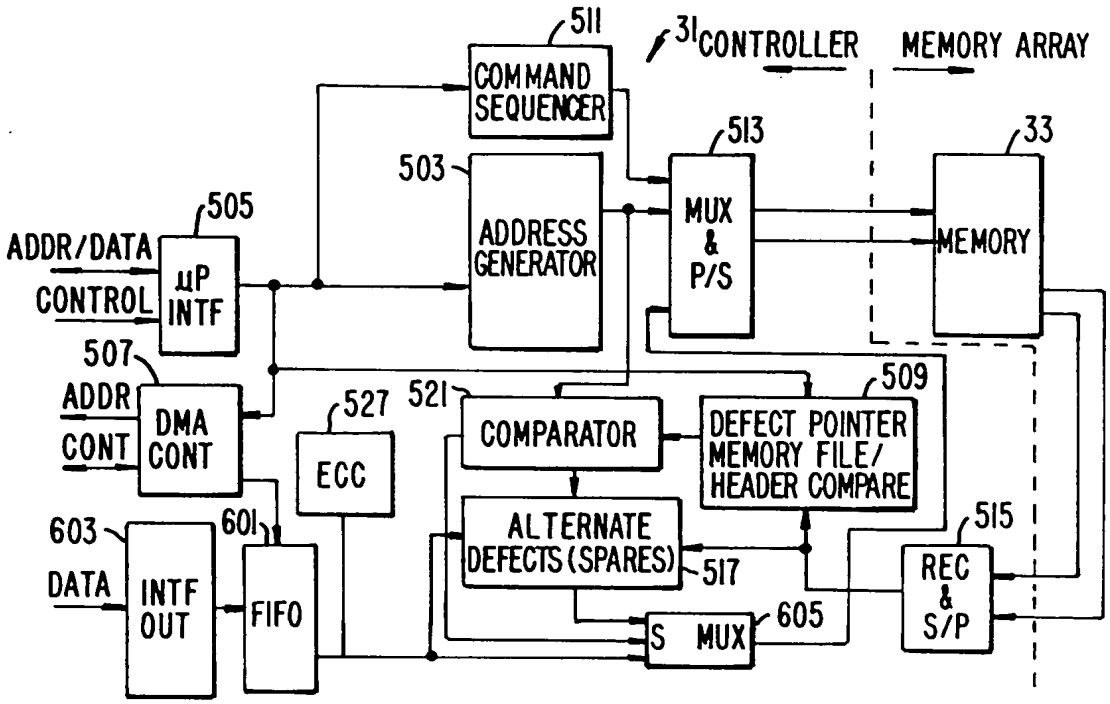
FIG._8.

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS



READ DATA PATH CONTROL

FIG._6.



WRITE DATA PATH CONTROL

FIG._7.

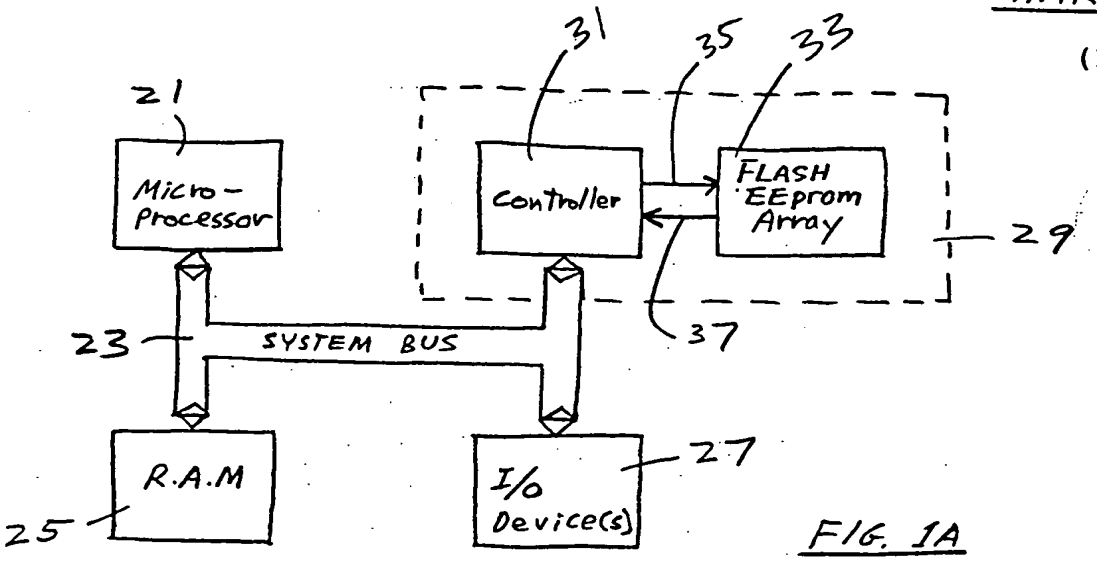

21
Micro-Processor
31
Controller
35
33
FLASH EEprom Array
29
23
SYSTEM BUS
37
R.A.M
25
I/O Device(s)
27

FIG. 1A

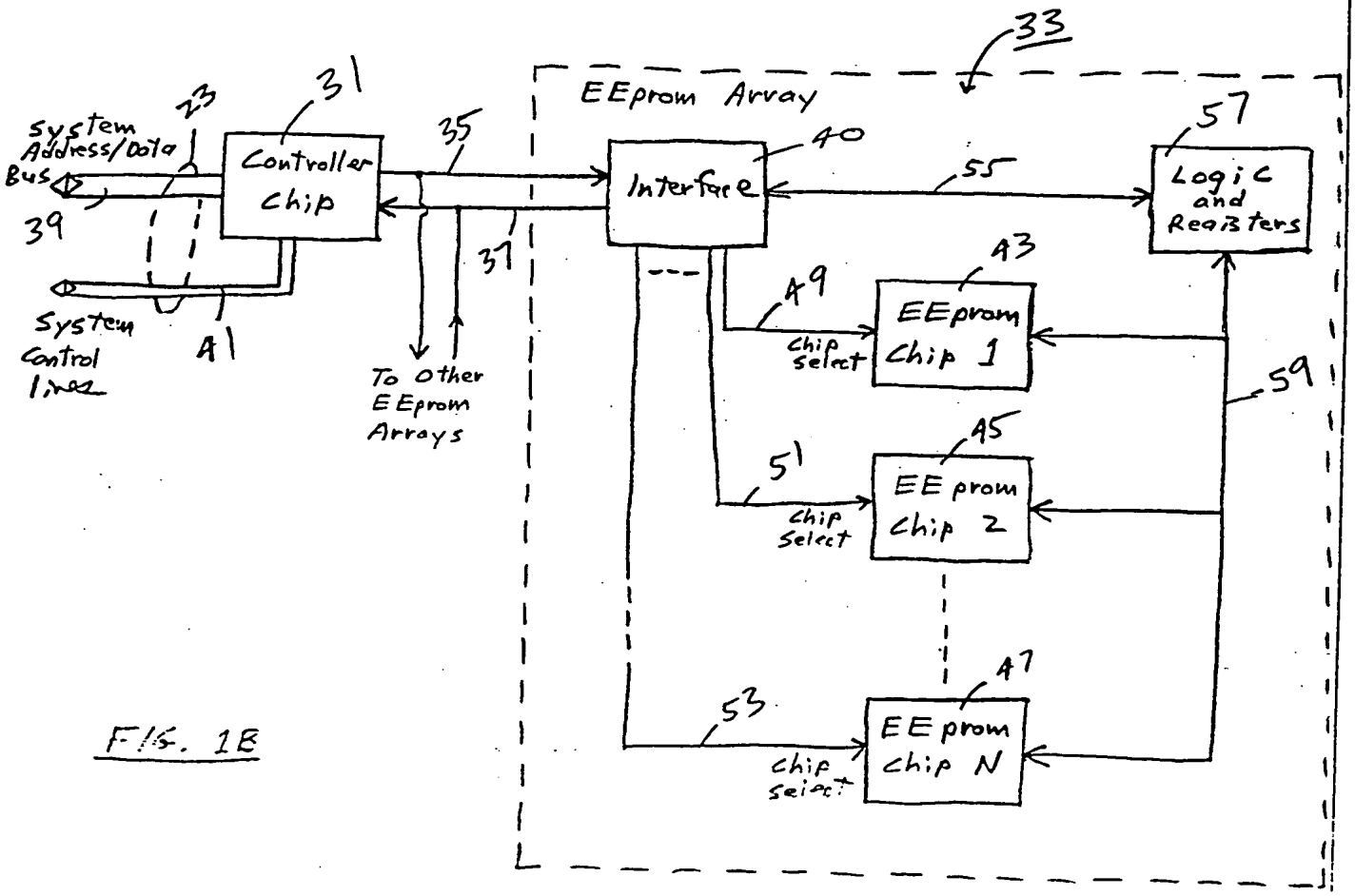

33
EEprom Array
System Address/Data Bus
23
39
31
Controller Chip
35
37
40
Interface
55
57
Logic and Registers
41
EEprom Chip 1
49
chip select
59
45
EE prom Chip 2
51
chip select
47
EE prom Chip N
53
chip select
System Control lines
43
To Other EEprom Arrays

FIG. 1B

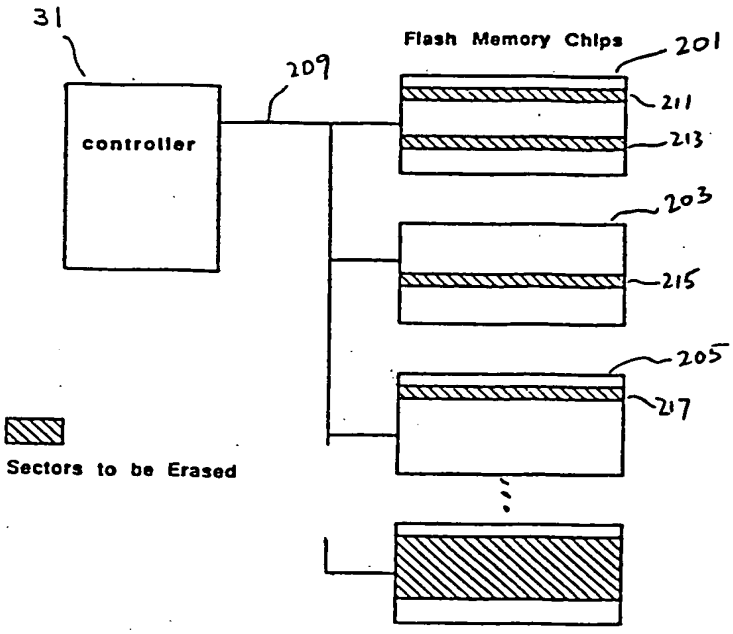


FIG_2

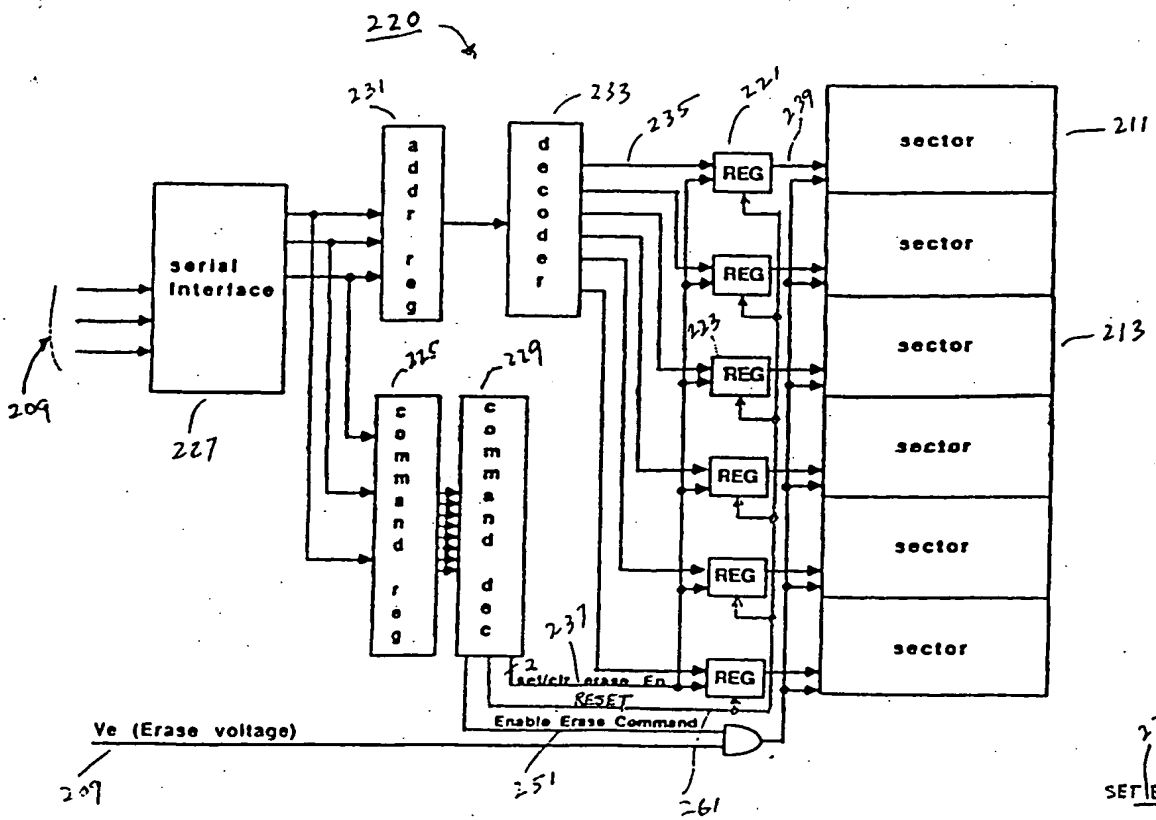


FIG_3A

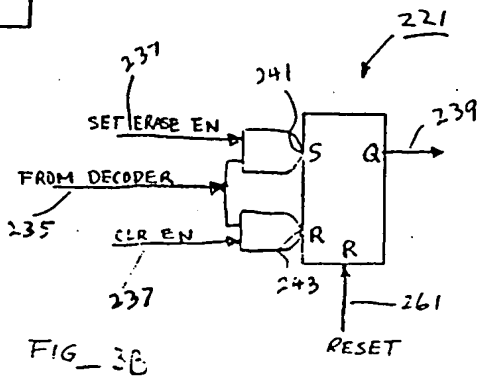


FIG_3B

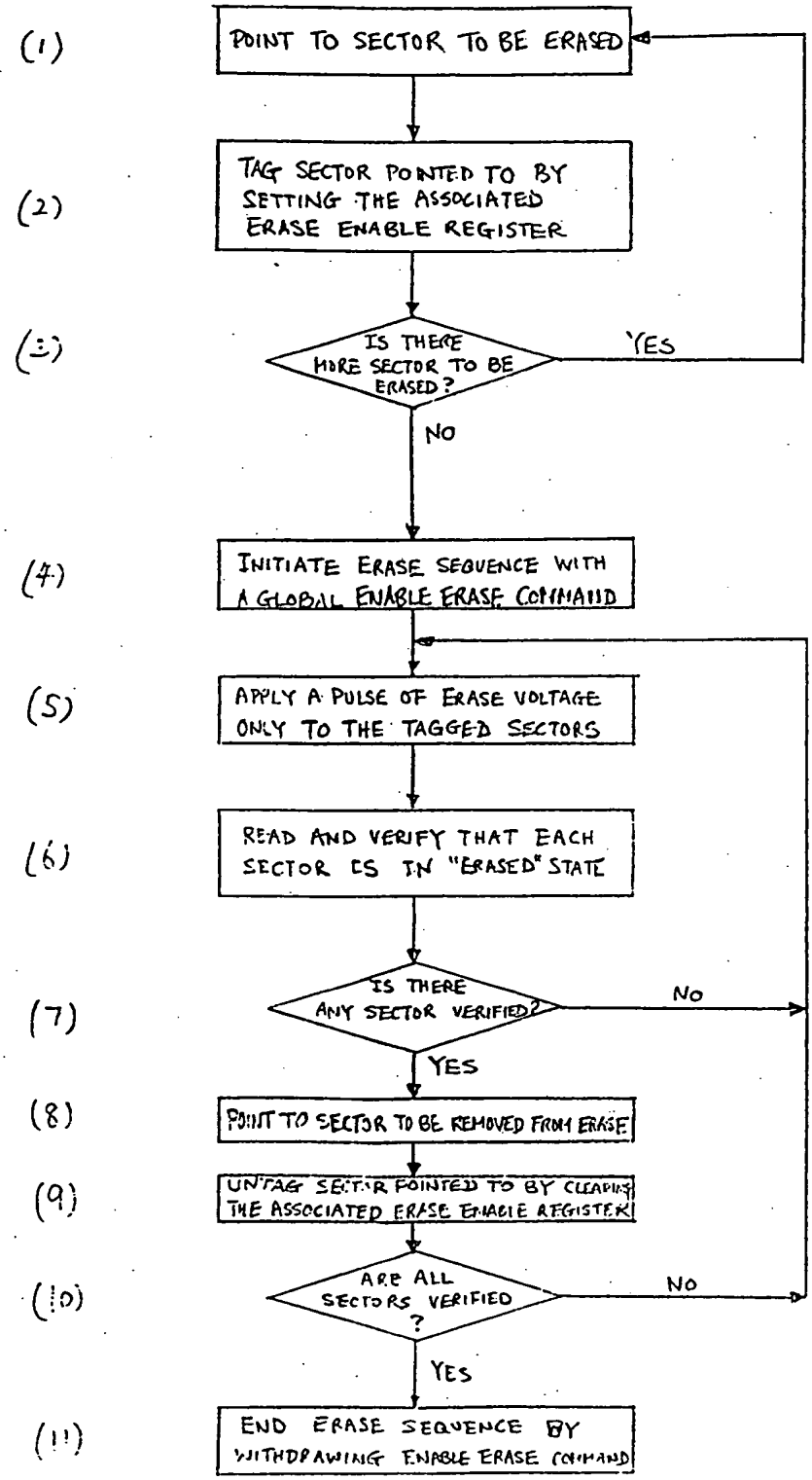
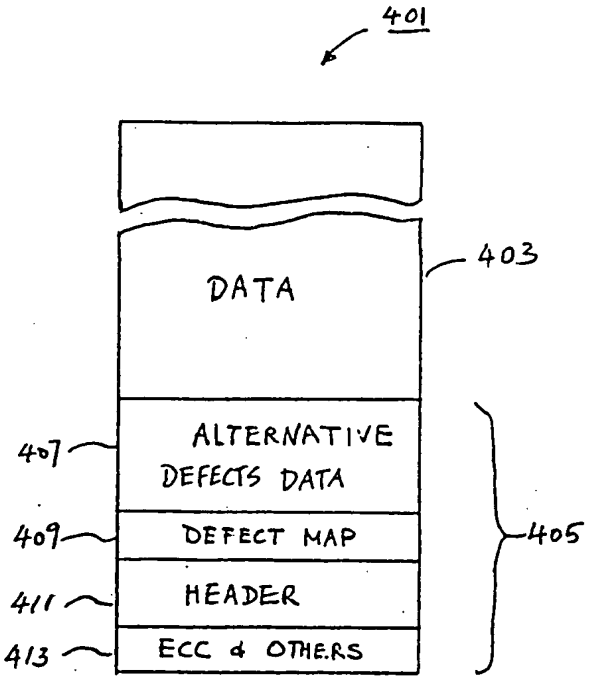

(1)
POINT TO SECTOR TO BE ERASED
(2)
TAG SECTOR POINTED TO BY SETTING THE ASSOCIATED ERASE ENABLE REGISTER
(3)
IS THERE MORE SECTOR TO BE ERASED?
YES
NO
(4)
INITIATE ERASE SEQUENCE WITH A GLOBAL ENABLE ERASE COMMAND
(5)
APPLY A PULSE OF ERASE VOLTAGE ONLY TO THE TAGGED SECTORS
(6)
READ AND VERIFY THAT EACH SECTOR IS IN "ERASED" STATE
(7)
IS THERE ANY SECTOR VERIFIED?
No
YES
(8)
POINT TO SECTOR TO BE REMOVED FROM ERASE
(9)
UNTAG SECTOR POINTED TO BY CLEARING THE ASSOCIATED ERASE ENABLE REGISTER
(10)
ARE ALL SECTORS VERIFIED ?
No
YES
(11)
END ERASE SEQUENCE BY WITHDRAWING ENABLE ERASE COMMAND

FIG_4



SECTOR PARTITION

FIG_5

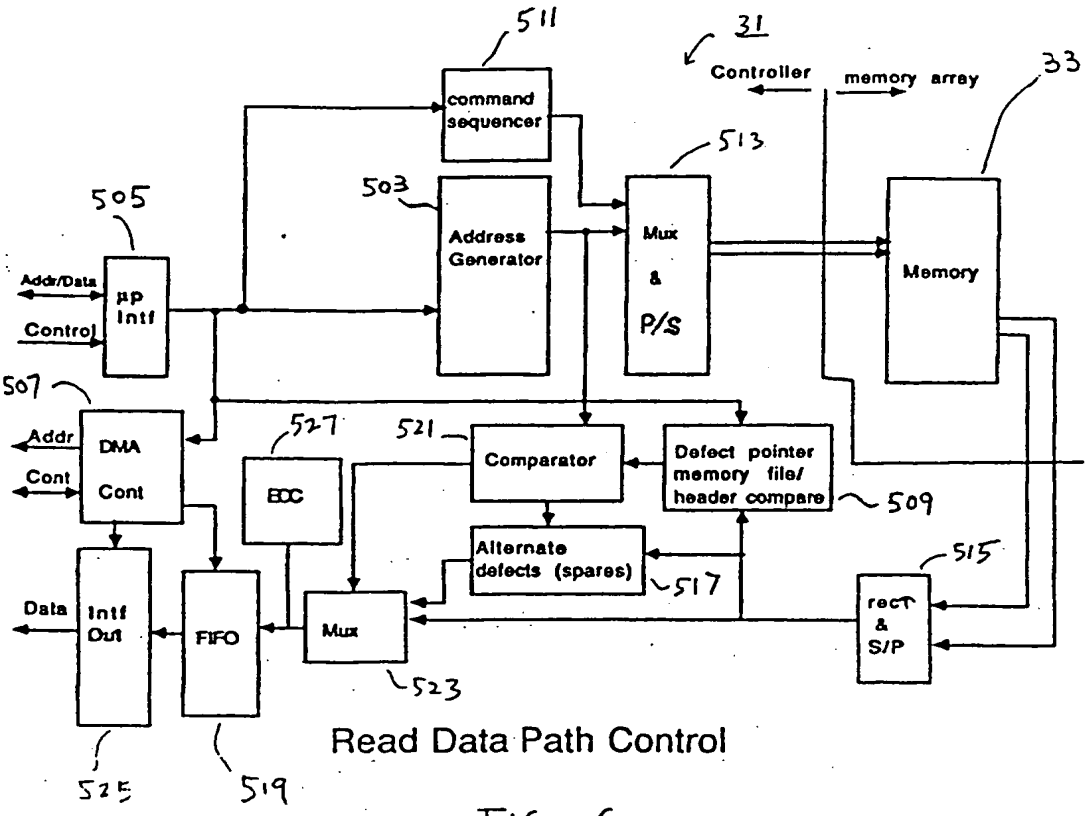

511
31
Controller
memory array
33
command sequencer
513
503
505
Address Generator
Mux & P/S
Memory
Addr/Data
µp Intf
Control
507
Addr
DMA Cont
Cont
527
521
Comparator
Defect pointer memory file/ header compare
509
ECC
Alternate defects (spares)
517
515
rect & S/P
Data
Intf Out
FIFO
Mux
523
525
519
Read Data Path Control

FIG_ 6

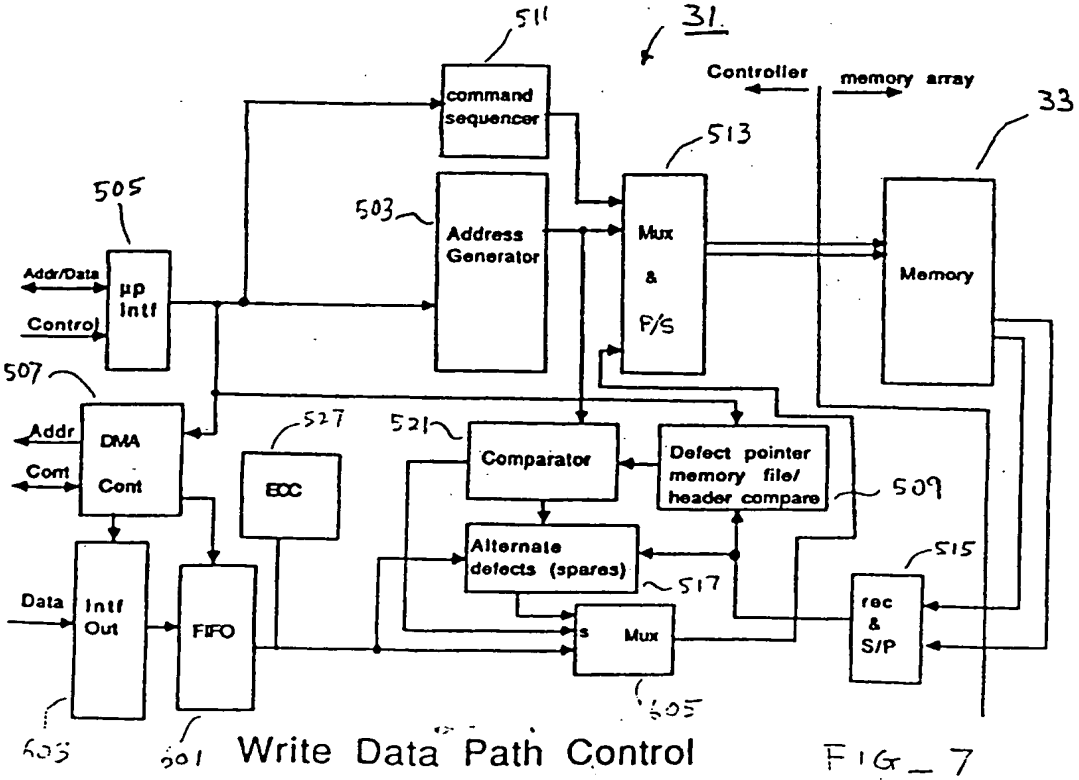

511
31
Controller
memory array
33
command sequencer
513
505
503
Address Generator
Mux & P/S
Memory
Addr/Data
µp Intf
Control
507
Addr
DMA Cont
Cont
527
521
Comparator
Defect pointer memory file/ header compare
509
ECC
Alternate defects (spares)
517
515
rec & S/P
Data
Intf Out
FIFO
s
Mux
505
503
501
Write Data Path Control

FIG_ 7

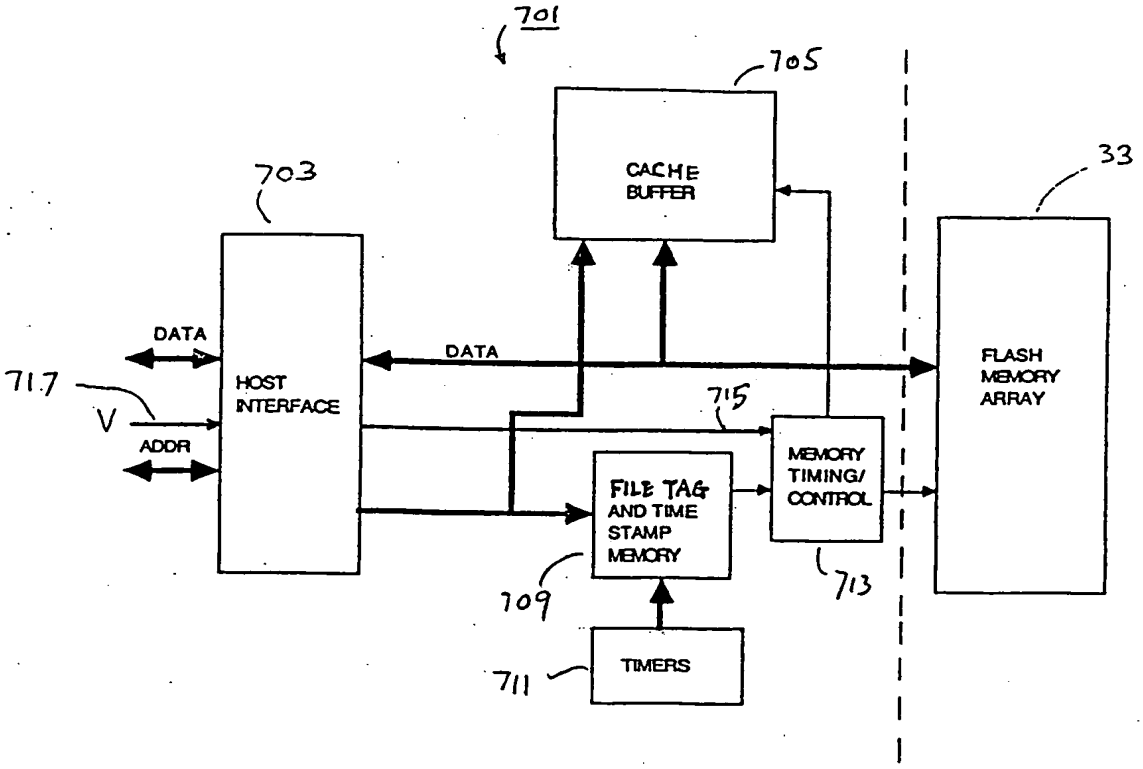

701
705
CACHE BUFFER
703
33
DATA
DATA
HOST INTERFACE
FLASH MEMORY ARRAY
717
V
ADDR
715
MEMORY TIMING/ CONTROL
FILE TAG AND TIME STAMP MEMORY
709
713
TIMERS
711

FIG. 8